Vacuum 172 (2020) 109047

Contents lists available at ScienceDirect

Vacuum

journal homepage: http://www.elsevier.com/locate/vacuum

Short communication

Polycrystalline Ge intermediate layer for Ge/Si wafer bonding and defect elimination in Si (SOI)-based exfoliated Ge film

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ARTICLE INFO

Keywords:
Ge/Si wafer bonding
Poly-Ge
By-products
Point defects

ABSTRACT

We report the Ge/Si wafer bonding with polycrystalline Ge (Poly-Ge) intermediate layer. The effect of the Poly-Ge layer fabricated by different methods on the transferring of the by-products at the bonded interface was investigated. The dependence of the bubble density on the Poly-Ge film thickness was also identified. Due to the high crystallinity of the Poly-Ge film fabricated by furnace, the gas formed at the bonded interface can be effectively absorbed, leading to the decrease of the bubble density. The exfoliation of the Si-based and SOI-based Ge film was successfully achieved by Smart-Cut™ technique. More importantly, the crystalline quality of the Ge film was improved by controlling the point defects in the exfoliated Ge film. Finally, the $FWHM_{XRD}$ of 60 arc sec for Si-based Ge film and the $FWHM_{XRD}$ of 111 arc sec for SOI-based Ge film, which are much lower than that of the epitaxial ones, were achieved.

In the past few years, many researchers focused on the investigation of Ge/Si epitaxial growth [1–3] and Ge/Si photoelectric device [4–6] due to the excellent infrared absorption properties of Ge material and the fact that the Ge material can be integrated with Si CMOS circuit. In addition, for Ge/Si single-photon avalanche photodiode (SPAD) [7–9], the Ge material can serve as the infrared absorption layer and the Si material (impact ionization coefficient ratio<0.1 [10], low excess noise) can serve as the multiplication layer to achieve the SPAD with low afterpulsing probability for near-infrared single-photon counting or quantum communication. Therefore, high-quality Ge/Si heterogeneous hybrid integration is needed for the achievement of high-performance photoelectric device.

Ge/Si heterogeneous hybrid integration is commonly based on the traditional Si-based Ge film epitaxial growth. The crystalline quality of the Ge film determines the properties of the photoelectric device. It is important to note that high-density threading dislocations (TDs) (10^7-10^9 cm^{-2} [11–13]) exist in the Si-based Ge film due to the 4.2% lattice mismatch between Ge and Si. This limits the further reduction of the dark current density of the Ge/Si device. Although many modified epitaxial methods [14–16] were proposed to decrease the TD density (TDD), the TDD is still difficult to be decreased to $<10^6$ cm^{-2}. Thus, the FWHM of the Ge(004) XRD peak of the epitaxial Ge film is commonly in the range of 200–400 arc sec [17,18]. Recently, some researchers proposed to fabricate high-quality Si-based Ge film by low-temperature Ge/Si wafer bonding [19–21]. The TDs can be eliminated at the bonded interface when low-temperature annealing was carried out due to the low threading rate of misfit dislocations [22]. However, low-temperature Ge/Si wafer bonding suffers from high-density bubbles at the Ge/Si bonded interface due to the hydrophilic reaction (Ge-OH + OH-Ge→Ge-O-Ge + H_2O and Ge + $2H_2O$→GeO_2+$2H_2$) at the bonded interface at present. This leads to the decrease of the effective area for the fabrication of the device. In addition, few previous works illustrated the exfoliation of Ge film on Si and SOI substrates by low-temperature Ge/Si wafer bonding and Smart-Cut™ technique. Moreover, the method for the improvement of the crystalline quality of the exfoliated Ge film has also not been reported previously.

In this paper, the polycrystalline Ge (poly-Ge) bonding layer was introduced to achieve a bubble-free Ge/Si bonded interface. The effect of the crystallinity of the poly-Ge film on the bubble evolution was identified. Based on the bubble-free Ge/Si wafer bonding, the Si-based and SOI-based Ge film were successfully exfoliated by Smart Cut™ technique. The surface etching and high-temperature annealing were

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https://doi.org/10.1016/j.vacuum.2019.109047
Received 29 September 2019; Received in revised form 25 October 2019; Accepted 28 October 2019
Available online 31 October 2019
0042-207X/

proposed to eliminate the point defects. Finally, ultrahigh-quality Si-based ($FWHM_{XRD} = 60''$) and SOI-based exfoliated Ge film ($FWHM_{XRD} = 111''$) were achieved. We believe that this method can be considered as a potential substitute of the epitaxy technique in the future for the fabrication of high-quality semiconductor thin film which has high lattice mismatch with its substrate, such as GeSn on Si or III-V group material on Si.

The (001)-oriented n^+-Si substrates (~0.001 Ω cm) and the SOI substrates with 220 nm thick n-type top Si layer ((001)-oriented, ~0.001 Ω cm) were cleaned with standard RCA process. After that a thin a-Ge layer was deposited on Si and SOI substrates by sputtering. The Si and SOI substrates were annealed at 600 °C for 5 min in the furnace to trigger the crystallization of a-Ge after a 100 nm thick SiO_2 capping layer was deposited on the a-Ge layer. For comparison, the annealing of the a-Ge film in the rapid thermal annealing (RTA) chamber was also carried out. After annealing, the SiO_2 capping layer was removed by HF solution. The (001)-oriented i-Ge (>30 Ω cm) substrates were degreased with acetone, alcohol, and DI water in the ultrasonic bath for 10 min, respectively. A part of the Ge substrates were directly bonded to the Ge layer on Si substrates, then the bonded samples were annealed at 300 °C for 30 h to enhance the bonding strength. Here, we name the samples with Ge layer annealed in RTA chamber as sample A and that annealed in the furnace as sample B. A part of the Ge substrates were implanted by H^+ with the dose of 5×10^{16} cm^2 and the energy of 150 keV to create a defective blistered region below the Ge surface (~1.2 μm below Ge surface). After that the implanted Ge substrates were bonded to the Ge layer (furnace) on Si and SOI substrates at room temperature. Then the bonded samples were firstly annealed at 150 °C under a force of 2 MPa for 1 h in the bonder. After that the samples were annealed at 100 °C for 1 h, 200 °C for 1 h, 300 °C for 1 h, and 400 °C for 1 h without force in N_2 atmosphere to trigger the exfoliation of the Ge film after the samples were taken out of the bonder. The heating rate of 5 °C/min was applied. The exfoliated Ge film was polished by chemical mechanical polishing (CMP) to smooth the Ge surface. Here, we name the polished Si-based Ge film as sample C and the polished SOI-based Ge film as sample D. The surface morphology was examined ex situ by atomic force microscope (AFM). The bonded interfaces were identified by C-mode scanning acoustic microscope (CSAM) with a frequency of 250 MHz. The crystalline quality of the Ge film was evaluated by Raman spectroscopy (532 nm) and x-ray diffraction (XRD) measurement.

Fig. 1(a)-(d) show the CSAM images of the Ge/Si bonded interfaces in sample A with different thickness of poly-Ge film. One can see that dense bubbles appear at the Ge/Si bonded interface when 30 nm thick poly-Ge film was inserted. This indicates that 30 nm thick poly-Ge fabricated by RTA cannot totally absorb the by-products (H_2 and H_2O) formed at the bonded interface. With the increase of the poly-Ge film thickness, the bubble density decreases. When the poly-Ge film thickness increases to 100 nm, some bubbles still exist at the bonded interface. The CSAM images of the Ge/Si bonded interfaces in sample B are shown in Fig. 1(e)-(h). One feature of particular interest is that few bubbles appear at the Ge/Si bonded interface with 30 nm thick poly-Ge film fabricated by furnace. This is very different from that in sample A. This indicates that the 30 nm thick poly-Ge fabricated by furnace can absorb most of the by-products at the bonded interface. With the increase of the poly-Ge film thickness, the bubble density shows changeless. A near-bubble-free Ge/Si bonded interface was achieved.

In order to clearly illustrate this phenomenon, we also fabricate the Si/Si bonded samples with poly-Ge film fabricated by RTA and furnace, respectively. The CSAM images of the Si/Si bonded interfaces with poly-Ge film fabricated by RTA are shown in Fig. 2(a)-(d). One can see that lots of bubbles also appear at the Si/Si bonded interface with 30 nm thick poly-Ge fabricated by RTA. With the increase of the poly-Ge film thickness, the density of small bubbles decreases. Only the big bubbles originate from the particles introduced during contact process appear at the bonded interface. For the samples with poly-Ge film fabricated by furnace, as shown in Fig. 2(e)-(f), the Si/Si bonded interface with 30 nm thick poly-Ge film is bubble-free. This is consistent with that in Ge/Si bonded interface in sample B.

Note that no bubbles appear at the Si/Si bonded interface, while some small bubbles still exist at the Ge/Si bonded interface with the same thickness of poly-Ge film fabricated by furnace. As we all know that the Ge substrate is difficult to be cleaned by inorganic solution due to the high etching rate of Ge wafer cleaned by these solutions. On the other hand, the organic cleaning always cannot absolutely clean the Ge surface. Thus, we believe that the appearance of the small bubbles at Ge/Si bonded interface is attributed to the fact that some particles still absorb on the Ge substrate after organic cleaning and the Si substrate is absolutely clean after RCA cleaning.

In order to reveal the different interface characteristics of Ge/Si bonded interface in sample A and sample B, the Raman spectrum and the XRD of the poly-Ge film were detected, as shown in Fig. 3(a) and (b), respectively. One can see that the Ge–Ge peak of the Ge film appears at ~300 cm^{-1}, indicating that the Ge film annealed in furnace has crystallized. However, for the Ge film annealed in RTA chamber, except the Ge–Ge peak at ~300 cm^{-1}, the Ge–Ge peak which represents the amorphous phase of the Ge film appear at ~280 cm^{-1}, suggesting that the Ge film annealed by RTA does not completely crystallized. This leads to the increase of the FWHM of the Ge–Ge peak at ~300 cm^{-1} (7.75–9.16 cm^{-1}). The XRD curves are shown in Fig. 3(b) to identify the crystalline characteristics of the poly-Ge film. One can see that the (111), (220), and (311) peaks of the Ge film appear at 28° for the Ge film annealed in furnace, while the (111) and (311) peaks become weak and

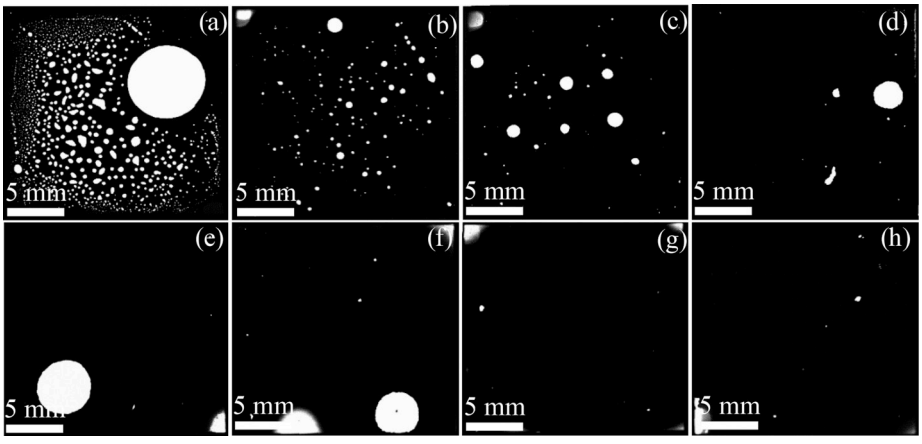

Fig. 1. CSAM images of the Ge/Si bonded interfaces (300 °C for 10 h) with (a) 30 nm, (b) 60 nm, (c) 80 nm, and (d) 100 nm thick poly-Ge film fabricated by RTA. CSAM images of the Ge/Si bonded interfaces (300 °C for 10 h) with (e) 30 nm, (f) 60 nm, (g) 80 nm, and (h) 100 nm thick poly-Ge film fabricated by furnace.

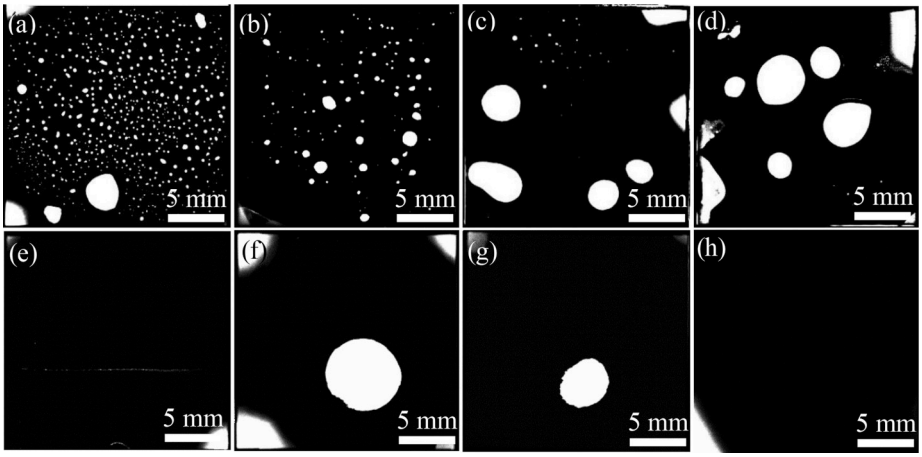

Fig. 2. CSAM images of the Si/Si bonded interfaces (300 °C for 10 h) with (a) 30 nm, (b) 60 nm, (c) 80 nm, and (d) 100 nm thick poly-Ge film fabricated by RTA. CSAM images of the Si/Si bonded interfaces (300 °C for 10 h) with (e) 30 nm, (f) 60 nm, (g) 80 nm, and (h) 100 nm thick poly-Ge film fabricated by furnace.

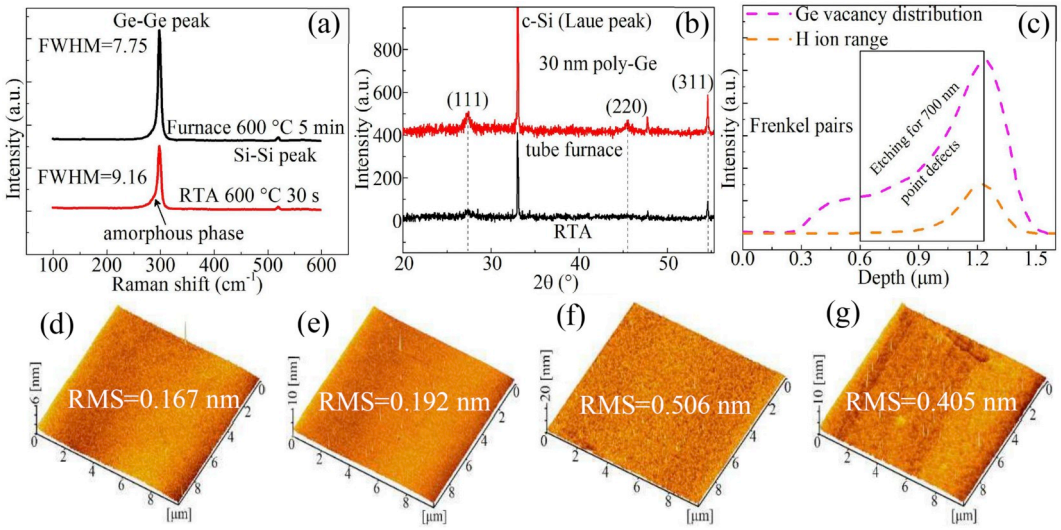

Fig. 3. (a) Raman spectrum of the poly-Ge film. (b) XRD curves of the poly-Ge film. (c) Simulation of the Ge vacancy distribution in Ge substrate after H^+ implantation. (d) and (e) AFM images of the Si-based and SOI-based Ge surface before etching, respectively. (f) and (g) AFM images of the Si-based and SOI-based Ge surface after etching, respectively.

the (220) peak disappears when the Ge film was annealed in RTA. This indicates that the crystalline quality of the poly-Ge film annealed in furnace is higher than that annealed in RTA. We can suggest that with the increase of the crystallinity of poly-Ge film, the number of the grain boundarys increases. The by-products at the bonded interface can be transferred out of the wafer by these grain boundarys, leading to the decrease of the bubble density.

After the investigation of the bubble evolution at the Ge/Si bonded interface, we select 30 nm thick poly-Ge film fabricated by furnace for the Si-based and SOI-based Ge film exfoliation. The XRD curves of the Si-based (sample C) and SOI-based Ge film (sample D) are shown in Fig. 4 (a) and (d), respectively. One can see that the FWHM of the Ge(004) peak of sample C and sample D is as low as 79 and 108 arc sec, respectively, which are much lower than that of the epitaxial ones. Note that the FWHM of the Ge(004) peak of sample C is lower than that of sample D. This may be due to the lower crystalline quality of the top Si layer than that of the Si substrate. Although the Ge(004) peak is narrow, however, the Ge(004) peak of the as-exfoliated Ge film is asymmetric. The shoulder peak at the left side of the Ge peak results from the interference effects between substrate and strained layers [23,24,25], which are created by the hydrogen implantation. And the lower half of the Ge peak is wide, stemming from the point defects in the Ge film formed by the H^+-implantation.

Ge vacancy distribution in Ge substrate after H^+ implantation was simulated, as shown in Fig. 3(c). One can see that the peak position of the H^+ concentration is located at 1.23 μm (Ge film thickness). The Ge vacancy (Frenkel pairs) induced by the H^+ implantation is mainly distributed in the range of 0.6–1.4 μm. In order to enhance the Ge film quality, the Ge film which contains point defects and non-uniform strain should be etched. The AFM images of the Ge surface of sample C and sample D before etching are shown in Fig. 3(d) and (e). One can see that the Ge surface is extremely smooth before etching, the RMS of both samples is below 0.2 nm. The AFM images of both samples after etched by reactive ion etching (RIE) with power of 100 W are shown in Fig. 3(f) and (g). One can see that after etching, the RMS of the Ge surface slightly increases, while the RMS is still lower (~0.5 nm). This is enough for the fabrication of photoelectric device. Fig. 4(b) and (e) show the XRD curves of the Si-based and SOI-based Ge film etched for 700 nm by reactive ion etching, respectively. One can see that the Ge(004) peak becomes symmetrical and the FWHM of the Ge peak is changeless after etching. This indicates that the defect region of the Ge film was etched and the quality of the Ge film was improved.

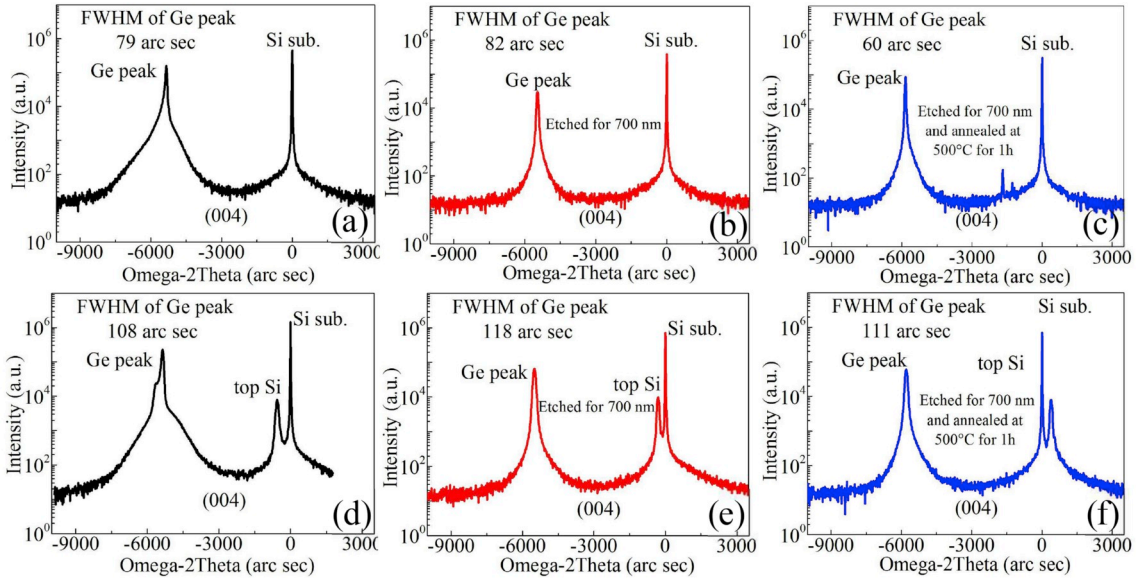

Fig. 4. XRD curves of the Si-based exfoliated Ge film (a) without post-treatment, (b) etched for 700 nm, and (c) etched for 700 nm and annealed at 500 °C for 1 h. XRD curves of the SOI-based exfoliated Ge film (a) without post-treatment, (b) etched for 700 nm, and (c) etched for 700 nm and annealed at 500 °C for 1 h.

As we all know that the impurities should be activated at high temperature (≥500 °C) to achieve ohmic contact for the fabrication of photoelectric device, thus we investigate the high-temperature characteristics of the exfoliated Ge film which has been etched for 700 nm, as shown in Fig. 4(c) and (f). One can see that the peak shape of the Ge (004) peak of the Ge film shows no change after the Ge film was annealed at 500 °C for 1 h. More importantly, the FWHM of the Ge peak of sample C decreases to 60 arc sec and that of sample D decreases to 111 arc sec after annealing. This may be attributed to the repairing of the point defects in the Ge film which was not etched, as shown in Fig. 3(c). The FWHM of 60 arc sec and the 111 arc sec is the lowest one at present for Si-based and SOI-based Ge film, respectively, suggesting that ultrahigh-quality exfoliated Ge film was achieved.

In summary, the Poly-Ge film fabricated by RTA and furnace was applied for Ge/Si wafer bonding. The bubble density at the Ge/Si bonded interface with Poly-Ge film fabricated by furnace is lower than that fabricated by RTA. The high crystallinity of the Poly-Ge film fabricated by furnace can be responsible for this phenomenon. With the increase of the Poly-Ge film thickness, the bubble density decreases. However, some small bubbles still exist at the bonded interface due to the introduction of small particles during the bonding process. The Si-based and SOI-based Ge film were successfully exfoliated by Poly-Ge bonding and Smart-Cut™ technique, and the point defects in the exfoliated Ge were eliminated by the etching of the defect region or by high-temperature annealing. Finally, high-quality Si-based and SOI-based Ge film which shows excellent high-temperature characteristics was achieved.

Acknowledgements

This work was supported by the National Natural Science Foundation of China (61534005, 61974122 and 11673019). General Armaments Department, People's Liberation Army of China (6140721040411). National Key Research and Development Program of China (2018YFB2200103).

References

[1] M.A. Wistey, Y.Y. Fang, J. Tolle, A.G. Chizmeshya, J. Kouvetakis, Chemical routes to Ge/Si (100) structures for low temperature Si-based semiconductor applications, Appl. Phys. Lett. 90 (8) (2007), 082108, https://doi.org/10.1063/1.2437098.

[2] A. Sakai, N. Taoka, O. Nakatsuka, S. Zaima, Y. Yasuda, Pure-edge dislocation network for strain-relaxed Si Ge/Si (001) systems, Appl. Phys. Lett. 86 (22) (2005) 221916, https://doi.org/10.1063/1.1943493.

[3] T.H. Loh, H.S. Nguyen, C.H. Tung, A.D. Trigg, G.Q. Lo, N. Balasubramanian, D. L. Kwong, S. Tripathy, Ultrathin low temperature SiGe buffer for the growth of high quality Ge epilayer on Si (100) by ultrahigh vacuum chemical vapor deposition, Appl. Phys. Lett. 90 (9) (2007), 092108, https://doi.org/10.1063/1.2709993.

[4] M. Kim, O. Olubuyide, J. Yoon, J. Hoyt, Selective epitaxial growth of Ge-on-Si for photodiode applications, ECS Trans. 16 (10) (2008) 837–847, https://doi.org/10.1149/1.2986843.

[5] M. Steglich, M. Oehme, T. Käsebier, M. Zilk, K. Kostecki, E.B. Kley, J. Schulze, A. Tünnermann, Ge-on-Si photodiode with black silicon boosted responsivity, Appl. Phys. Lett. 107 (5) (2015), 051103, https://doi.org/10.1063/1.4927836.

[6] X. Sun, J. Liu, L.C. Kimerling, J. Michel, High-performance, tensile-strained Ge p-i-n photodetectors on a Si platform, Opt. Lett. 34 (8) (2009) 1198–1200, https://doi.org/10.1063/1.2037200.

[7] N.J. Martinez, M. Gehl, C.T. Derose, A.L. Starbuck, A.T. Pomerene, A.L. Lentine, D. C. Trotter, P.S. Davids, Single photon detection in a waveguide-coupled Ge-on-Si lateral avalanche photodiode, Opt. Express 25 (14) (2017) 16130–16139, https://doi.org/10.1364/OE.25.016130.

[8] Z. Lu, Y. Kang, C. Hu, Q. Zhou, H.D. Liu, J.C. Campbell, Geiger-mode operation of Ge-on-Si avalanche photodiodes, IEEE J. Quantum Electron. 47 (5) (2011) 731–735, https://doi.org/10.1109/JQE.2011.2110637.

[9] R.E. Warburton, G. Intermite, M. Myronov, P. Allred, D.R. Leadley, K. Gallacher, D. J. Paul, Neil J. Pilgrim, L.J.M. Lever, Z. Ikonic, R.W. Kelsall, Ge-on-Si single-photon avalanche diode detectors: design, modeling, fabrication, and characterization at wavelengths 1310 and 1550 nm, IEEE Trans. Electron Devices 60 (11) (2013) 3807–3813, https://doi.org/10.1109/TED.2013.2282712.

[10] A. Pauchard, Y. Kang, P. Mages, M. Bitter, D. Sengupta, Z. Pan, S. Hummel, Y.H. Lo, Optical Fiber Communication Conference (WV7), Optical Society of America, 2002, March.

[11] H.C. Luan, D.R. Lim, K.K. Lee, K.M. Chen, J.G. Sandland, K. Wada, L.C. Kimerling, High-quality Ge epilayers on Si with low threading-dislocation densities, Appl. Phys. Lett. 75 (19) (1999) 2909–2911, https://doi.org/10.1063/1.125187.

[12] A. Sakai, K. Sugimoto, T. Yamamoto, M. Okada, H. Ikeda, Y. Yasuda, S. Zaima, Reduction of threading dislocation density in SiGe layers on Si (001) using a two-step strain-relaxation procedure, Appl. Phys. Lett. 79 (21) (2001) 3398–3400, https://doi.org/10.1063/1.1419037.

[13] H.Y. Yu, J.H. Park, A.K. Okyay, K.C. Saraswat, Selective-area high-quality germanium growth for monolithic integrated optoelectronics, IEEE Electron. Device Lett. 33 (4) (2012) 579–581, https://doi.org/10.1109/LED.2011.2181814.

[14] L. Vivien, J. Osmond, J.M. Fédéli, D. Marris-Morini, P. Crozat, J.F. Damlencourt, E. Cassan, S. Laval, 42 GHz pin Germanium photodetector integrated in a silicon-on-insulator waveguide, Opt. Express 17 (8) (2009) 6252–6257, https://doi.org/10.1364/OE.17.006252.

[15] X. Sun, J. Liu, L.C. Kimerling, J. Michel, Direct gap photoluminescence of n-type tensile-strained Ge-on-Si, Appl. Phys. Lett. 95 (1) (2009), 011911, https://doi.org/10.1063/1.3170870.

[16] M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, E.A. Fitzgerald, Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing, Appl. Phys. Lett. 72 (14) (1998) 1718–1720, https://doi.org/10.1063/1.121162.

[17] S. Ke, Y. Ye, J. Wu, Y. Ruan, X. Zhang, W. Huang, C. Li, S. Chen, Interface characteristics of different bonded structures fabricated by low-temperature a-Ge

wafer bonding and the application of wafer-bonded Ge/Si photoelectric device, J. Mater. Sci. 54 (3) (2019) 2406–2416, https://doi.org/10.1007/s10853-018-3015-8.

[18] Z. Zhou, C. Li, H. Lai, S. Chen, J. Yu, The growth, characterization and electronic device applications of GaAs/Si, J. Cryst. Growth 310 (10) (2008) 2508–2513, https://doi.org/10.1557/PROC-145-261.

[19] F. Gity, K. Yeol Byun, K.H. Lee, K. Cherkaoui, J.M. Hayes, A.P. Morrison, C. Cindy, B. Corbett, Characterization of germanium/silicon p-n junction fabricated by low temperature direct wafer bonding and layer exfoliation, Appl. Phys. Lett. 100 (9) (2012), 092102, https://doi.org/10.1063/1.3688174.

[20] K.Y. Byun, P. Fleming, N. Bennett, F. Gity, P. McNally, M. Morris, I. Ferain, C. Colinge, Comprehensive investigation of Ge-Si bonded interfaces using oxygen radical activation, J. Appl. Phys. 109 (12) (2011) 123529, https://doi.org/10.1063/1.3601355.

[21] H. Kanbe, M. Miyaji, T. Ito, Ge/Si heterojunction photodiodes fabricated by low temperature wafer bonding, APEX 1 (7) (2008), 072301, https://doi.org/10.1143/apex.1.072301.

[22] R. Hull, J.C. Bean, L.J. Peticolas, B.E. Weir, K. Prabhakaran, T. Ogino, Misfit dislocation propagation kinetics in Ge_xSi_{1-x}/Ge (100) heterostructures, Appl. Phys. Lett. 65 (3) (1994) 327–329, https://doi.org/10.1063/1.113023.

[23] I.P. Ferain, K.Y. Byun, C.A. Colinge, S. Brightup, M.S. Goorsky, Low temperature exfoliation process in hydrogen-implanted germanium layers, J. Appl. Phys. 107 (5) (2010), 054315, https://doi.org/10.1063/1.3326942.

[24] X. Yu, J. Kang, R. Zhang, M. Takenaka, S. Takagi, Characterization of ultrathin-body Germanium-on-insulator (GeOI) structures and MOSFETs on flipped Smart-Cut™ GeOI substrates, Solid State Electron. 115 (2016) 120–125, https://doi.org/10.1016/j.sse.2015.08.021.

[25] C. Miclaus, M.S. Goorsky, Strain evolution in hydrogen-implanted silicon, J. Phys. D Appl. Phys. 36 (10A) (2003) A177, https://doi.org/10.1088/0022-3727/36/10a/336.